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Description

Method for producing an integrated circuit with a rewiring device and corresponding integrated circuit

The present invention relates to a method for producing an integrated circuit with a rewiring device, and a corresponding integrated circuit.

CSPs (chip scale packages) have to date predominantly been constructed on prefabricated substrate strips. In accordance with known CSP technologies based on a substrate, such as Tessera µBGA (micro ball grid array), for example, the rewiring (redistribution lines) or at least parts thereof are already integrated into the prefabricated substrate. Such a rewiring present on the substrate is then contact-connected by means of bonding wires or TAB bonding to an integrated circuit or a chip. The production of the substrate requires complicated and expensive process steps which increase the costs for the substrate. Furthermore, the production and the subsequent process steps are effected with a low degree of parallelism, e.g. in panels or strips with fewer than 150 chips. Both causes have hitherto prevented a further lowering of the production costs of CSPs. Fan-out rewirings can also be generated by means of CSP technologies based on a substrate, for example by means of the BGA technology.

Wafer level package technologies (WLP) likewise provide a cost-effective technology for producing chip scale packages (CSPs), but without being able to provide fan-out rewirings. The wafer level package technologies utilize as a basis the front end wafer, on which the thin-film technique is used in order to produce the fan-in rewiring, the insulation layers, such as e.g. a solder resist layer, and the solder balls. Although the

technology steps used in this case for metallization, i.e. sputtering and electrodeposition, for structure production, i.e. photolithography, and for producing protection layers, i.e. spin coating, are cost-intensive, the individual costs per chip can be kept low on account of the high degree of parallelism (entire wafer with up to 1000 chips). In addition, in the future more cost-effective printing technologies will increasingly replace the expensive photolithographic process steps. New printing technologies will make it possible to produce a mask technique using the printing method, which can be used for the highly accurate contact connection of contact pads on a wafer, typical contact pad spacings comprising 130 µm, for example, and typical pad openings comprising 60 µm. Printing processes can thus be used for structure production of rewiring devices or insulation wires on a new panel. However, the WLP production cannot be used to produce fan-out rewirings, i.e. rewirings which project beyond the chip edge.

Therefore, the object of the present invention is to provide a method for producing an integrated circuit with a rewiring device and likewise such an integrated circuit in a cost-effective manner.

According to the invention, this object is achieved by means of the method for producing an integrated circuit with a rewiring device as specified in Claim 1 and by means of the integrated circuit with a rewiring device according to Claim 19.

The idea on which the present invention is based essentially consists in suitably combining process steps of wafer level package technologies together with substrate-based CSP technologies. Thus, prefabricated substrates with rewiring layers are avoided, rather a rewiring device is only produced during the production

process of the chip scale package on a simple, large-area substrate with a high degree of parallelism.

In the present invention, the problem mentioned in the introduction is solved in particular by virtue of the fact that a method for producing an integrated circuit with a rewiring device is provided, having the following steps: provision of a carrier device with predefined or subsequently patterned cutouts; application of at least one integrated circuit upside down to the carrier device in such a way that the defined cutouts of the carrier device are located above at least one connection device of the integrated circuit; application of an insulation device to that side of the carrier device which is not covered by the integrated circuit, omitting the at least one connection device in the cutout; application of the patterned rewiring device to the insulation device; application of a patterned solder resist device to the patterned rewiring device; and patterned application of solder balls on regions which are not covered by the patterned solder resist device.

What is advantageous in this case is that the rewiring or parts thereof do not already have to be provided on a substrate or a carrier device from the outset. In addition, a fan-out design is possible, i.e. rewirings which project beyond the chip edge. Furthermore, the size of the carrier device may considerably exceed that of conventional substrates, e.g. with integrated rewiring layers. In particular, said size may also exceed the wafer area since panel sizes of 600 mm x 400 mm can be realized even without considerable cost expenditure. What is more, such a carrier device or panel does not have to be round like a wafer, for example, but rather may also be formed in rectangular fashion in a manner adapted to the chip geometry.

In addition to these directly cost-effective advantages, the present invention affords further beneficial advantages in that greater freedom in the choice of materials is available, that production of multichip units, so-called multichip modules, with integrated circuits or chips of different form and size is also made possible since the population of the carrier device is not restricted to uniform chips, and in that there is a possibility for the multi-die test and burn-in after complete processing, similar to the wafer level test (WLT) and wafer level burn-in (WLBI) already known.

Advantageous developments and improvements of the respective subject matter of the invention are found in the subclaims.

In accordance with one preferred development, the carrier device is a film in which the at least one cutout is present, or is subsequently produced, in the form of a stamped-out hole.

In accordance with a further preferred development, before the application of the integrated circuit, an adhesive is applied to the carrier device.

In accordance with a further preferred development, the carrier device is clamped in a clamping-in device such as e.g. a frame.

In accordance with a further preferred development, a multiplicity of integrated circuits are applied to the carrier device by means of a placement device, such as e.g. a pick-and-place tool.

In accordance with a further preferred development, a protection device is applied above the carrier device and the at least one integrated circuit applied.

In accordance with a further preferred development, the protection device is applied in an injection-molding method, in a printing process or a potting process and/or is subsequently cured.

In accordance with a further preferred development, a polymer is applied as the insulation device.

In accordance with a further preferred development, the insulation device is printed on or produced in a photolithographic process.

In accordance with a further preferred development, the patterned rewiring device is applied to the insulation device by means of the following steps: application of a carrier metallization to the insulation device; application and patterning of a mask on the carrier metallization; application of a conductor track metallization in regions of the carrier metallization which are not covered by the patterned mask; removal of the mask; and patterning of the carrier metallization in accordance with the conductor track metallization structure.

In accordance with a further preferred development, the carrier metallization is sputtered on and/or the mask is patterned photolithographically and/or the conductor track metallization is electrochemically plated and/or the carrier metallization is patterned in an etching step.

In accordance with a further preferred development, the solder resist device has a polymer.

In accordance with a further preferred development, the solder resist device is printed on.

In accordance with a further preferred development, the solder balls are applied in patterned fashion in a printing process and are subsequently reliquefied, preferably in a furnace, and solder balls are formed.

In accordance with a further preferred development, a multiplicity of integrated circuits on a carrier device, after the application of the solder balls, are separated into individual integrated circuits or groups of integrated circuits.

In accordance with a further preferred development, a multiplicity of integrated circuits with rewiring devices on the carrier device undergo a functional test prior to the separation.

In accordance with a further preferred development, the patterned rewiring device is patterned in such a way that it extends laterally beyond the chip edge.

In accordance with a further preferred development, multichip modules are formed, which preferably have different individual ICs.

An exemplary embodiment of the invention is illustrated in the drawings and is explained in more detail in the description below.

In the figures:

Figures 1-10 show a diagrammatic cross-sectional view of individual stages in the production process of an integrated circuit with rewiring device for elucidating an embodiment of the present invention; and

Figure 11 shows a diagrammatic cross-sectional view of an integrated circuit with rewiring device for elucidating an embodiment of the present invention in an enlarged illustration.

In the figures, identical reference symbols designate identical or functionally identical constituent parts.

Figure 1 illustrates a carrier device 10 provided with vertically continuous cutouts 11. The carrier device 10 or the substrate is a film or a flexible substrate, for example, the cutouts 11 being present e.g. in the form of stamped holes.

In accordance with Figure 2, the carrier device 10 with the cutouts 11 provided therein is provided with an adhesive 12 at the top side and clamped into a frame 13. Said frame 13 may have both round and angular forms and its size is limited only by the requirements in the subsequent process steps, such as, for example, printing technique, photolithography. In particular, the size of the carrier device 10 can extend to wafer size (200 mm, 300 mm), but also beyond that.

In a subsequent process step, in accordance with Figure 3, integrated circuits 14 are applied and positioned upside down on the carrier device 10 with adhesive 12 applied thereto in such a way that connection devices 15, such as contact pads for example, of the integrated circuit 14 are located in the region of the cutouts 11. In this case, the distance between the integrated circuits 14 or the distance between the cutouts 11 is preferably chosen in such a way that a rewiring layer that is subsequently to be created, on that side of the substrate film 10 or carrier device which is not provided with adhesive 12, can be led laterally beyond the chip

edge. The integrated circuits 14 can be applied and positioned by means of a placement device, such as a pick-and-place tool, for example.

For the protection of the integrated circuits 14, in accordance with Figure 4, a protection device 16 is preferably provided above the integrated circuits 14 on the side remote from the contact pads 15. Consequently, if appropriate before the production of a rewiring device, the entire chip assembly comprising a multiplicity of integrated circuits 14 on the carrier device 10 is provided with a protection device 16 by means of an injection-molding method or another potting or printing method, which protection device is subsequently cured. A rigid composite, similar to a wafer, can be obtained as a result.

Figure 5 shows the arrangement in accordance with Figure 4 after the application of an insulation device 17 on that side of the carrier device 10 which is not provided with integrated circuits 14, no insulation device 17 being applied over the connection devices 15 or contact pads in the cutouts of the carrier device 11 [sic]. The insulation device 17, preferably a polymer, is applied e.g. photolithographically or in a printing method.

A rewiring device 18, 19 is thereupon applied on said insulation device 17 in accordance with Figure 6. The rewiring device 18, 19 has electrically conductive sections 18 or conductor track sections and electrically insulating sections 19, the conductor track sections 18 being at least partly contact-connected to the contact pads 15. The rewiring metallization 18 of the rewiring device 18, 19 is preferably formed as follows: sputtering of a carrier metallization onto the insulation device 17; application and photolithographic patterning of a mask (not illustrated); electrochemical deposition of the

conductor track metallization 18 on the sputtered-on carrier metallization in sections not covered by the mask; removal of the mask; and etching of the carrier metallization patterned in such a way as the conductor track metallization 18. In addition, an electrically nonconductive material 19 may be provided laterally between the conductor track sections 18. Consequently, the rewiring layer 18, 19 is produced by means of thin-film or printing technology on that side of the carrier device 10 or substrate film which is not provided with the integrated circuits 14.

After a further method step, in accordance with Figure 7, a solder resist device 20 has been applied to the rewiring device 18, 19 in patterned fashion preferably in a printing process. Said solder resist device 20, preferably comprising a polymer, is patterned in such a way that cutouts are provided over predetermined sections 21 of the conductor track metallization 18 of the rewiring device 18, 19.

In accordance with Figure 8, solder 22 is applied in the cutouts 21 in the solder resist device 20 over the predetermined sections 21 of the conductor track metallization 18, preferably in a printing process.

In the arrangement in accordance with Figure 9, these solder balls 22 have been reliquefied, preferably in a reflow furnace, and subsequently cooled, thereby forming solder balls 22'.

Following Figure 10, the chip composite comprising a plurality of integrated circuits 14 has been divided into separated integrated circuits 23 with fan-out rewiring device 18, 19, 20.

The arrangement in accordance with Figure 11 shows in detail such a separated integrated circuit 23 which has been produced in accordance with the method according to the invention. By means of the procedure described, in a manner similar to that in the case of a prefabricated substrate, i.e. with rewiring layers, a rewiring technology is provided which, however, according to the present invention, can be produced with a high degree parallelism and can thus be produced cost-effectively. This technology according to the invention utilizes WLP processes, fan-out designs now also being possible. The integrated circuits 23 with rewiring device are preferably separated in a dicer.

Although the present invention has been described above on the basis of a preferred exemplary embodiment, it is not restricted thereto, but rather can be modified in diverse ways.

Thus, in particular, the materials explained (polymer, ...) are to be regarded as by way of example. Furthermore, the rewiring device 18, 19, 20, 22 can also be produced in an alternative way.

List of reference symbols

10	Carrier device, preferably flexible, e.g. film
11	Cutout in carrier device, e.g. stamped
12	Adhesive
13	Frame
14	Integrated circuit
15	Connection device, e.g. contact pads
16	Protection device
17	Insulation device, preferably a polymer
18	Conductive device, e.g. conductor track metallization
19	Nonconductive device
20	Solder resist device, preferably a polymer
21	Section of the conductor track metallization that is not covered by solder resist device (cutout in polymer)
22	Solder ball
22′	Reliquefied solder ball
23	Separated integrated circuit with fan-out rewiring device